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ACCELERATOR AND RADIATION PHYSICS encompasses radiation shielding design and strategies for hadron therapy accelerators, neutron facilities and laser based accelerators. A fascinating article describes detailed transport theory and its application to radiation transport. Detailed information on planning and design of a very high energy proton accelerator can be obtained from the article on radiological safety of J-PARC. Besides safety for proton accelerators, the book provides information on radiological safety issues for electron synchrotron and prevention and preparedness for

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radiological emergencies. Different methods for neutron dosimetry including LET based monitoring, time of flight spectrometry, track detectors are documented along with newly measured experimental data on radiation interaction with dyes, polymers, bones and other materials. Design of deuteron accelerator, shielding in beam line hutches in synchrotron and 14 MeV neutron generator, various radiation detection methods, their characterization, dose mapping procedures and simulation of radiation environment are also discussed.

This book describes image processing research based on the morphology of the objects in an image and a VLSI design of a Cellular Logic Processing Element for a real-time processor pipeline. The field of image processing has spawned a number of special parallel computer architectures: the Square (SIMD), Processor Array, the Pyramid, the Linear Processor Array (or scan line array) and the Processor Pipeline. This book features a classification of low-level image processing operations, reviews some intermediate level algorithms, and gives a short introduction into computer architecture used for image and digital signal processing. Morphology-based processing images is introduced by treating cellular logic operations such as skeletonization as hit-or-miss transformations. This approach can be extended to images of higher dimensions than two and a method is described to construct hit-or-miss masks for the skeletonization of these images. In the second part of the book a study is performed on the speed bottlenecks that can be found in the main architectural

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groups followed by the description of a method for the structured design of integrated, digital hardware. The VLSI design of a CMOS Processing Element for the real-time processing of binary images and the board level design of a scalable processor pipeline for a real-time low-level processing of grey value images is described in detail. Finally, a computer architecture for low and intermediate processing of two and three dimensional images is proposed.

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